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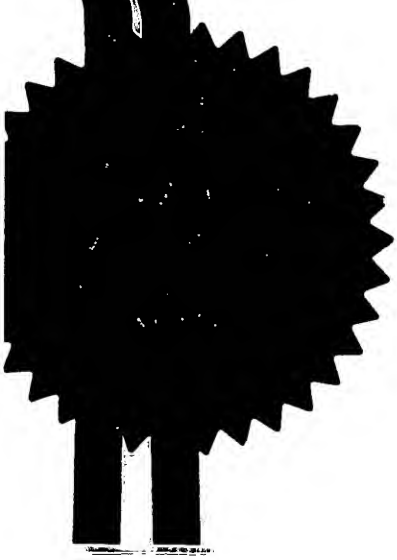

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Dated 20 December 2001

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Patents Form 1/77

Patents Act 1977
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The Patent Office

24JAN01 E600362-6/D01063
P01/7700 0.00-0101784.7

1/77

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24 JAN 2001
NEWPORT

Request for grant of a patent

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The Patent Office

Cardiff Road
Newport
South Wales
NP9 1RH

1. Your reference — JSR.P51327GB

2. Patent application number *(The Patent Office will fill in this part)* — **0101784.7** — 24 JAN 2001

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

Mitel Semiconductor Limited
Cheney Manor
Swindon
Wilts SN2 2QW

Patents ADP number *(if you know it)* 7387442001

If the applicant is a corporate body, give the country/state of its incorporation

4. Title of the invention — Amplifier

5. Name of your agent *(if you have one)*

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

Marks & Clerk
4220 Nash Court
Oxford Business Park South
Oxford
OX4 2RU

Patents ADP number *(if you know it)* 7271125001 ✓

6. If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or of each of these earlier applications and *(if you know it)* the or each application number

Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7. If this application is divided or otherwise derived from an earlier UK application, give the number and the filing date of the earlier application

Number of earlier application	Date of filing *(day / month / year)*

8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
b) there is an inventor who is not named as an applicant, or
c) any named applicant is a corporate body.
See note (d))

Yes

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	None
Description	9 ✓
Claim *(s)*	3 ✓
Abstract	1 ✓
Drawing *(s)*	4 ✓

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Priority documents	No
Translations of priority documents	No
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	1 ✓
Request for preliminary examination and search *(Patents Form 9/77)*	1 ✓
Request for substantive examination *(Patents Form 10/77)*	No
Any other documents *(please specify)*	No

11. I/We request the grant of a patent on the basis of this application.

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Date 23 January 2001

12. Name and daytime telephone number of person to contact in the United Kingdom: John S. Robinson - 01865 397900

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Patents Form 7/77

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24 JAN 2001
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Statement of inventorship and of right to grant of a patent

The Patent Office

Cardiff Road
Newport
South Wales
NP9 1RH

1. Your reference JSR.P51327GB

2. Patent application number *(if you know it)* **0101784.7** 24 JAN 2001

3. Full name of the or of each applicant
Mitel Semiconductor Limited

4. Title of the invention
Amplifier

5. State how the applicant *(s)* derived the right from the inventor *(s)* to be granted a patent
By virtue of employment

6. How many, if any, additional Patents Forms 7/77 are attached to this form? *(see note (c))* None

7. I/We believe that the person *(s)* named over the page *(and on any extra copies of this form)* is/are the inventor *(s)* of the invention which the above patent application relates to.

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Date
23 January 2001

8. Name and daytime telephone number of person to contact in the United Kingdom
John S. Robinson - 01865 397900

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Enter the full names, addresses and postcodes of the inventors in the boxes and underline the surnames

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Reminder

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AMPLIFIER

The present invention relates to an amplifier. Such an amplifier may, for example, be used at radio or intermediate frequencies, for example within a radio tuner. The present invention also relates to a radio tuner including such an amplifier.

According to a first aspect of the invention, there is provided an amplifier comprising a first long tail pair of transistors, a second long tail pair of transistors, and a current source for setting the tail currents of the first and second long tail pairs in a predetermined ratio, the current source comprising: at least one first bipolar transistor whose collector forms a first current source output, whose base is connected to a bias voltage source, and whose emitter is connected via a first resistance to a supply input; and a second bipolar transistor whose collector forms a second current source output, whose base is connected to the bias voltage source, and whose emitter is connected via a second resistance to the emitter of the first transistor.

The at least one first transistor may comprise a plurality of parallel-connected transistors.

The value of the second resistance may be substantially equal to:

$$\frac{Vt.\lambda}{I} \ln\left(\frac{\lambda}{n}\right)$$

Where ln is the natural logarithm, I is the output current of the first current source output, Vt is the thermal voltage, λ is the predetermined ratio, and n is the number of transistors forming the first transistor.

The first and second long tail pairs may have outputs connected to cross-connected first and second differential pairs of transistors.

The first long tail pair may comprise third and fourth transistors whose input terminals are connected to first and second inputs, respectively, of the amplifier and whose common terminals are connected via third and fourth resistances, respectively, to the first current source output. The third and fourth transistors may be bipolar transistors, the second amplifier input may be connected at signal frequencies to a common line, and the value of the third resistance may be substantially equal to the value of the fourth resistance plus (Zs/β_1), where Zs is a source impedance to which the first amplifier input is to be connected and β_1 is the current gain of the third transistor.

The second long tail pair may comprise fifth and sixth transistors whose input terminals are connected to first and second inputs, respectively, of the amplifier, whose common terminals are connected via fifth and sixth resistances, respectively, to the second source output, and whose output terminals are connected to output terminals of the fourth and third transistors, respectively. The fifth and sixth transistors may be bipolar transistors and the value of the fifth resistance may be substantially equal to the value of the sixth resistance plus (Zs/β_2), where β_2 is the current gain of the fifth transistor.

The second amplifier input may be connected to the common line by a capacitor.

According to a second aspect of the invention, there is provided an amplifier comprising: a first current source; a first bipolar transistor having a base for connection to a signal source having a source impedance Zs and an emitter connected via a first resistance to the first current source; and a second bipolar transistor having a base connected at signal frequencies to a common line and an emitter connected via a second resistance to the first current source, the value of the first resistance being substantially equal to the value of the second resistance plus (Zs/β_1), where β_1 is the current gain of the first transistor.

The amplifier may comprise: a second current source; a third bipolar transistor having a base connected to the base of the first transistor, an emitter connected via a third resistance to the second current source, and a collector connected to the collector of the second transistor; and a fourth bipolar transistor having a base connected to the base of

the second transistor, an emitter connected via a fourth resistance to the second current source, and a collector connected to the collector of the first transistor, the value of the third resistance being substantially equal to the value of the fourth resistance plus (Zs/β_2), where β_2 is the current gain of the first transistor.

The base of the second transistor may be connected to the common line by a capacitor.

According to a third aspect of the invention, there is provided a radio tuner including an amplifier according to the first or second aspect of the invention.

The invention will be further described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a circuit diagram of a transconductance amplifier to which the present invention may be applied;

Figure 2 is a circuit diagram of the current sources used in the amplifier of Figure 1;

Figure 3 is a circuit diagram of a twin current source for use in the invention;

Figure 4 is a circuit diagram of an amplifier constituting an embodiment of the invention; and

Figure 5 is a circuit diagram of the amplifier shown in Figure 4 but modified for receiving a single-ended input.

The transconductance amplifier shown in Figure 1 is of a type which is suitable for use as the first stage or low noise amplifier (LNA) of a radio frequency tuner, for example for receiving radio frequency input signals from a cable distribution network or from a satellite or terrestrial aerial. This transconductance stage is not an embodiment of the invention but is shown to illustrate a problem which the invention overcomes.

Low noise amplifiers are required to have a low noise figure while maintaining a high IIP3 or third order intermodulation performance. The transconductance amplifier shown in Figure 1 comprises two individual transconductance amplifier stages which are cross-connected so as to reduce intermodulation distortion. The first or main stage comprises a long tail pair of bipolar transistors T3 and T4 whose bases are connected to differential inputs IN+ and IN-, respectively. The emitters of the transistors T3 and T4 are connected via resistors R3 and R4, respectively, to one terminal of a constant current source CC1 whose other terminal is connected to ground. The constant current source CC1 supplies a current I_1.

The other or subsidiary stage likewise comprises a long tail pair of bipolar transistors T5 and T6 whose bases are connected to the differential inputs IN+ and IN-, respectively. The emitters of the transistors T5 and T6 are connected via resistors R5 and R6, respectively, to a second constant current source CC2 which supplies a tail current I_2. The cross-coupling of the main and subsidiary stages is achieved by connecting the collector of the transistor T5 to the collector of the transistor T4 and by connecting the collector of the transistor T6 to the collector of the transistor T3 so that the stage outputs are out of phase and the output of the subsidiary stage in the form of the differential collector current is subtracted from the output of the main stage.

The transconductance of the main stage comprising the transistors T3 and T4 is approximated by the following expression:

$$gm1.v+\alpha.v^3$$

where gm1 is the linear component of the transconductance, α is the coefficient of the third order part of the transconductance and v is the input voltage.

Similarly, to a good approximation, the transconductance of the subsidiary stage is given by:

$$gm2.v+\alpha.v^3$$

Where gm2 is the linear part of the stage transconductance. The transconductance of the whole transconductance amplifier is given by the difference between the transconductances of the individual stages, namely:

$$gm1.v+\alpha.v^3-gm2.v-\alpha.v^3=(gm1-gm2)v$$

The main and subsidiary stages are designed such that the third order transconductance terms cancel each other out whereas the linear terms are substantially different so that the difference between them is non-zero. In practice, it is possible to make the transconductance gm1 of the main stage much greater than the transconductance gm2 of the subsidiary stage so that the final transconductance of the whole amplifier is less than that of the main stage by only a small percentage. Typically, the value of each of the resistors R5 and R6 is one tenth of the value of each of the resistors R3 and R4 and the tail current I_2 of the subsidiary stage is one hundrenth of the tail current I_1 of the main stage. This results in a loss of gain (compared with that of the main stage alone) of about 2% but provides a very substantial increase in the inter modulation performance or IIP3.

In order for a good performance to be achieved in practice, the ratio of the currents I_1 and I_2 must be defined and maintained to a high degree of accuracy. This creates difficulties because of the need to maintain the ratio $I_1 : I_2$ at one hundred.

Figure 2 illustrates a conventional way of achieving such a large current ratio. The two current sources CC1 and CC2 are connected to a common bias voltage source 1, which supplies a substantially constant bias voltage Vbias. This first constant current source CC1 comprises ten bipolar transistors 11-20 connected in parallel with their bases connected to the bias voltage source 1, their emitters connected via a resistor 21 to ground, and their collectors connected together to form the output of the current source.

The second current source CC2 comprises a single transistor 22 whose collector forms the current source output, whose base is connected to the bias voltage source 1, and whose emitter is connected via a chain of ten series-connected resistors 23-32 to ground. The value of each of the resistors 23-32 is equal to the value of the resistor 21.

The twin current source of Figure 2 in fact achieves a current ratio of 10:1 but illustrates the difficulty in that the current-setting resistances in the emitter circuits have to have values which are in the same ratio as the desired currents. The current-setting resistors for the second current source CC2 thus occupy a very large area, for example of an integrated circuit in which the amplifier is formed.

Figure 3 shows a twin current source which does not suffer from such disadvantages, requiring only a relatively small area of silicon for fabrication. This arrangement comprises a bias voltage source 1 of the same type as shown in Figure 2 connected to the bases of transistors $T1_1$, $T1_2$ and T2. The part of the twin current source supplying the larger current I_1 comprises one or more transistors, illustrated in this particular embodiment as two parrallel-connected transistors $T1_1$ and $T1_2$. These transistors have bases connected to the bias voltage source 1, emitters connected via a resistor R1 to ground or any appropriate common or power supply line, and collectors connected together and forming the output for the larger current I_1.

The smaller current I_2 is supplied by the collector of the transistor T2, whose base is connected to the bias voltage source 1 and whose emitter is connected to a first terminal of a resistor R2, whose second terminal is connected to the emitters of the transistors $T1_1$ and $T1_2$ and to the resistor R1.

This twin current source makes use of a mismatch in transistor geometries in order to generate the different currents I_1 and I_2. The voltage drop across the base/emitter junction of the transistor T2 and the resistor R2 is equal to the base/emitter voltage of the transistors $T1_1$ and $T1_2$, that is :

$$Vbe_{T2}+I_2.R=Vbe_{T1}$$

where R is the value of the resistor R2. The collector current of the transistors $T1_1$ and $T1_2$ is given by:

$$Vbe_{T1} = Vt.\ln\left(\frac{I_1}{I_s}\right)$$

Where Vt is the thermal voltage, ln is the natural logarithm and Is is the saturation current.

A similar expression applies to the transistor T2 and this allows the base/emitter junction voltage drops to be replaced as follows:

$$I_2.R = Vt.\ln\left(\frac{I_1}{2.I_s}\right) - Vt.\ln\left(\frac{I_2}{I_s}\right)$$

This may be simplified by replacing the ratio I_1/I_2 with λ to give:

$$\frac{I_1.R}{\lambda} = Vt.\ln\left(\frac{\lambda}{2}\right)$$

which may be rewritten as:

$$R = \frac{\lambda}{I_1}\ Vt.\ln\left(\frac{\lambda}{2}\right)$$

Figure 4 illustrates an embodiment of the present invention in the form of an LNA for use as the first stage of a radio frequency tuner and incorporating the variable gain circuitry of an automatic gain control (AGC) circuit. The amplifier comprises a transconductance amplifier of the type illustrated in Figure 1 but in which the current sources CC1 and CC2 are replaced by the twin current source shown in Figure 3. The collectors of the transistors T3 and T6 are connected to the emitters of differentially

connected transistors T7 and T8 whose bases are connected to differential inputs AGC+ and AGC- for receiving a gain control voltage for controlling the gain of the LNA. The collector of the transistor T7 is connected via a load resistor R7 to a supply line vcc whereas the collector of the transistor T8 is connected directly to the supply line vcc. The collectors of the transistors T4 and T5 are similarly connected to the emitters of differentially connected transistors T9 and T10 whose bases are connected to the control voltage inputs AGC+ and AGC-, respectively. The collector of the transistor T9 is connected via a load resistor R8 to the supply line vcc whereas the collector of the transistor T10 is connected directly to the supply line vcc. Differential output signals of the LNA are generated across the load resistors R7 and R8 and are supplied to subsequent stages of the tuner, such as to a frequency changer.

As described hereinbefore, in a typical implementation of the LNA shown in Figure 4, the main stage current I_1 is required to be one hundred times the value of the subsidiary stage current I_2. This may be achieved in a typical implementation with the resistors R1 and R2 having values of 10 ohms and 24 ohms, respectively, the transistor T1 having an emitter area twenty times that of the transistor T2 (or comprising twenty parallel-connected transistors, each of the same size as the transistor T2), and the currents I_1 and I_2 being 40 and 1 milliamp, respectively.

The LNA shown in Figure 4 can readily be implemented on or as part of an integrated circuit and does not require and excessively large area of the substrate for fabrication. The amplifier has a gain and noise figure similar to those of conventional amplifiers but can achieve an improvement in IIP3 typically of 15 dB. Furthermore, such improvement in performance can be maintained over a large temperature range, in particular throughout the whole permissable operating temperature range of an integrated circuit. The twin current source maintains the required ratio of currents I_1:I_2 throughout the temperature range but the actual currents vary throughout the temperature range so as to compensate for other temperature-related effects and maintain the improvement in IIP3.

The amplifier shown in Figure 4 is intended for use with balanced or differential inputs supplied to its input terminals IN+ and IN-. However, it is common for the input to such an amplifier to be single-ended and the amplifier 5 may be connected for operation with such a single-ended input source. In this case, as shown in Figure 5, the amplifier has a single input IN and the bases of the transistors T4 and T6 are connected to ground via a capacitor 2. In particular, the capacitor 2 has a relatively low impedance for all signal frequencies which may be supplied to the input IN but isolates the bases of the transistors T4 and T6 from ground for direct current so as to prevent interference with base biasing arrangements (not shown). The input IN is intended to be connected to a signal source, such as a cable distribution network or aerial, having a well-defined characteristic source impedance.

The presence of the source impedance introduces an offset because the effective transconductance of the amplifier is unbalanced. However, this can be compensated by making the value of the emitter resistor R5 slightly larger than the value of the emitter resistor R6 and by making the value of the emitter resistor R3 slightly larger than the value of the emitter resistor R4. In particular, the value of each of the resistors R3 and R5 is made greater than the value of the resistor R4 and R6, respectively, by the amount Zs/β, where Zs is the source impedance of the signal source connected to the input IN and β is the current gain of the transistor T3 or T5 as appropriate. This offsetting of the emitter resistor values provides a further improvement in both IIP3 and IIP2 for single-ended inputs as compared with no offsetting of the emitter degeneration resistors.

CLAIMS:

1 An amplifier comprising a first long tail pair of transistors, a second long tail pair of transistors, and a current source for setting the tail currents of the first and second long tail pairs in a predetermined ratio, the current source comprising: at least one first bipolar transistor whose collector forms a first current source output, whose base is connected to a bias voltage source, and whose emitter is connected via a first resistance to a supply input; and a second bipolar transistor whose collector forms a second current source output, whose base is connected to the bias voltage source, and whose emitter is connected via a second resistance to the emitter of the first transistor.

2 An amplifier as claimed in claim 1 in which the at least one first transistor comprises a plurality of parallel-connected transistors.

3 An amplifier as claimed in claim 1 or 2 in which the value of the second resistance is substantially equal to:

$$\frac{Vt.\lambda}{I}\ln\left(\frac{\lambda}{n}\right)$$

where ln is the natural logarithm, I is the output current of the first current source output, Vt is the thermal voltage, λ is the predetermined ratio, and n is the number of transistors forming the first transistor.

4 An amplifier as claimed in any one of the preceding claims, in which the first and second long tail pairs have outputs connected to cross-connected first and second differential pairs of transistors.

5 An amplifier as claimed in any one of the preceding claims, in which the first long tail pair comprises third and fourth transistors whose input terminals are connected to first and second inputs, respectively, of the amplifier and whose common terminals are connected via third and fourth resistances, respectively, to the first current source output.

6 An amplifier as claimed in claim 5, in which the third and fourth transistors are bipolar transistors, the second amplifier input is connected at signal frequencies to a common line, and the value of the third resistance is substantially equal to the value of the fourth resistance plus (Zs/β_1), where Zs is a source impedance which the first amplifier input is to be connected and β_1 is the current gain of the third transistor.

7 An amplifier as claimed in claim 5 or 6, in which the second long tail pair comprises fifth and sixth transistors whose input terminals are connected to the first and second inputs, respectively, of the amplifier, whose common terminals are connected via fifth and sixth resistances, respectively, to the second current source output, and whose output terminals are connected to output terminals of the fourth and third transistors, respectively.

8 An amplifier as claimed in claim 7 when dependent of claim 6, in which the fifth and sixth transistors are bipolar transistors and the value of the fifth resistance is substantially equal to the value of the sixth resistance plus (Zs/β_2), where β_2 is the current gain of the fifth transistor.

9 An amplifier comprising: a first current source; a first bipolar transistor having a base for connection to a signal source having a source impedance Zs and an emitter connected via a first resistance to the first current source; and a second bipolar transistor having a base connected at signal frequencies to a common line and an emitter connected via a second resistance to the first current source, the value of the first resistance being substantially equal to the value of the second resistance plus (Zs/β_1), where β_1 is the current gain of the first transistor.

11 An amplifier as claimed in claim 10, comprising: a second current source; a third bipolar transistor having a base connected to the base of the first transistor, an emitter connected via a third resistance to the second current source, and a collector connected to the collector of the second transistor; and a fourth bipolar transistor having a base connected to the base of the second transistor, an emitter connected via a fourth

resistance to the second current source, and a collector connected to the collector of the first transistor, the value of the third resistance being substantially equal to the value of the fourth resistance plus (Zs/β_2), where β_2 is the current gain of the third transistor.

12 An amplifier as claimed in claim 10 or 11, in which the base of the second transistor is connected to the common line by a capacitor.

13 A radio tuner including an amplifier as claimed in any one of the preceding claims.

ABSTRACT
AMPLIFIER

A radio frequency amplifier of improved intermodulation performance is provided by connecting the first and second transconductance amplifiers (T3, T4, T5, T6, R3, R4, R5, R6) in antiphase so that third order intermodulation products cancel each other but the reduction in gain is relatively small. The transconductance stages comprise long tail pairs of transistors (T3, T4, T5, T6) provided with tail current sources formed by transistors (T1, T2) whose bases are connected to a bias voltage source 1. The first transistor (T1) has an emitter connected via a resistor (R1) to ground. The second transistor (T2) has an emitter connected via another resistor (R2) to the emitter of the first transistor (T1).

(Figure 4)

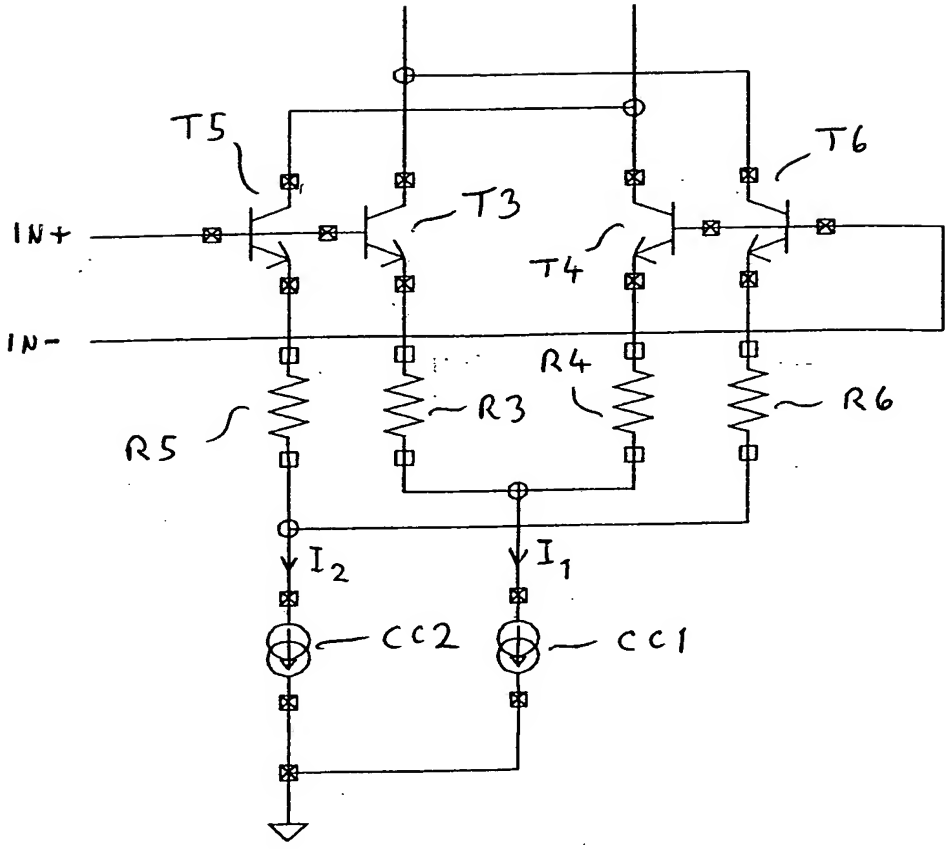


Fig 1

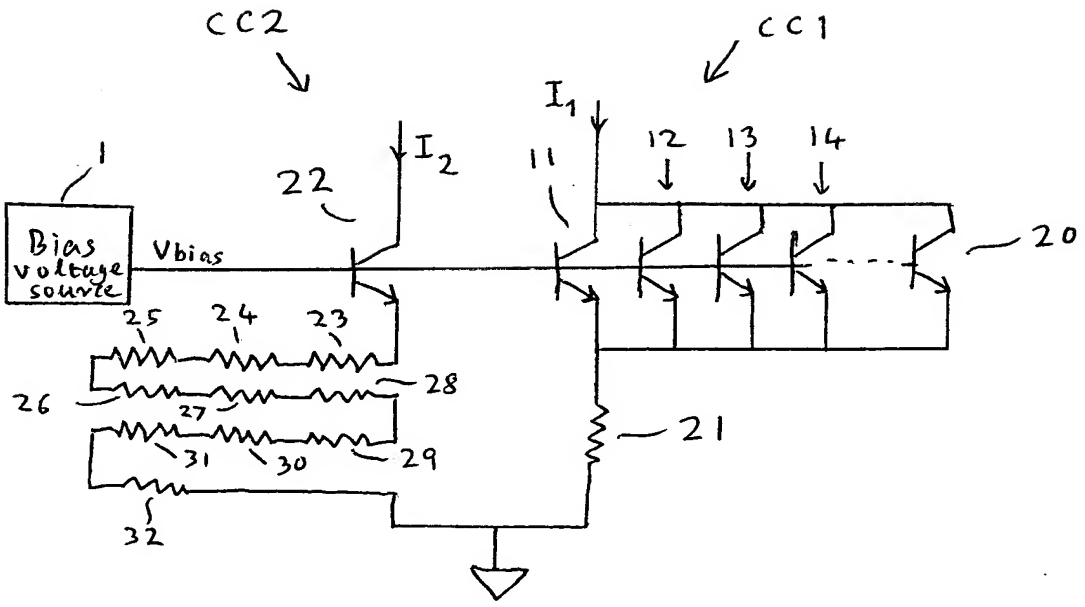
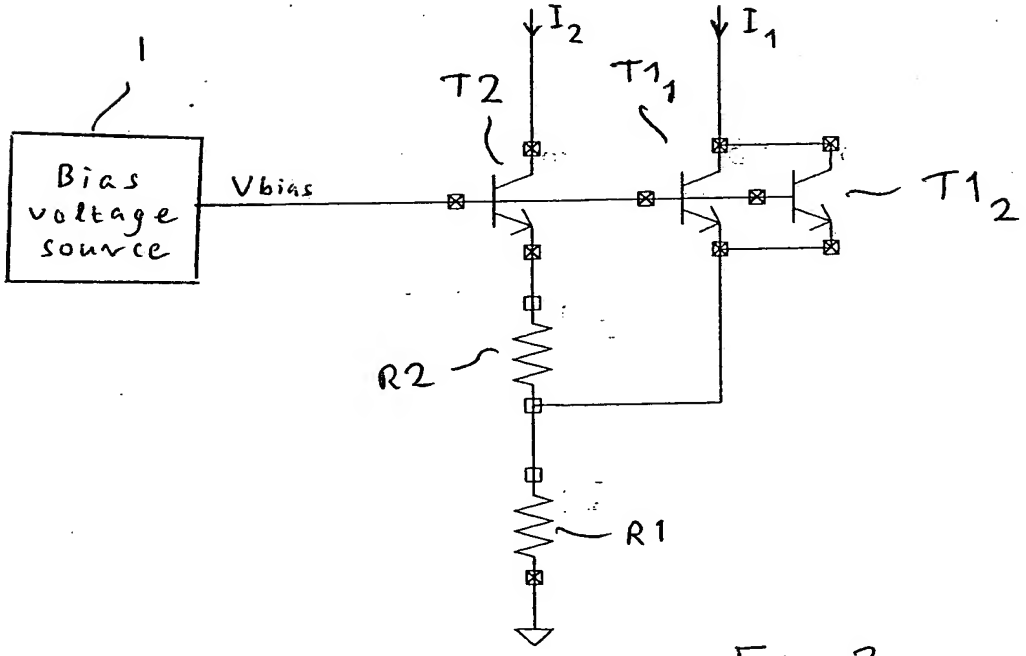

CC2
CC1
I_1
I_2
1
22
11
12
13
14
Bias voltage source
Vbias
20
25
24
23
26
28
27
21
31
30
29
32

Fig 2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I_1
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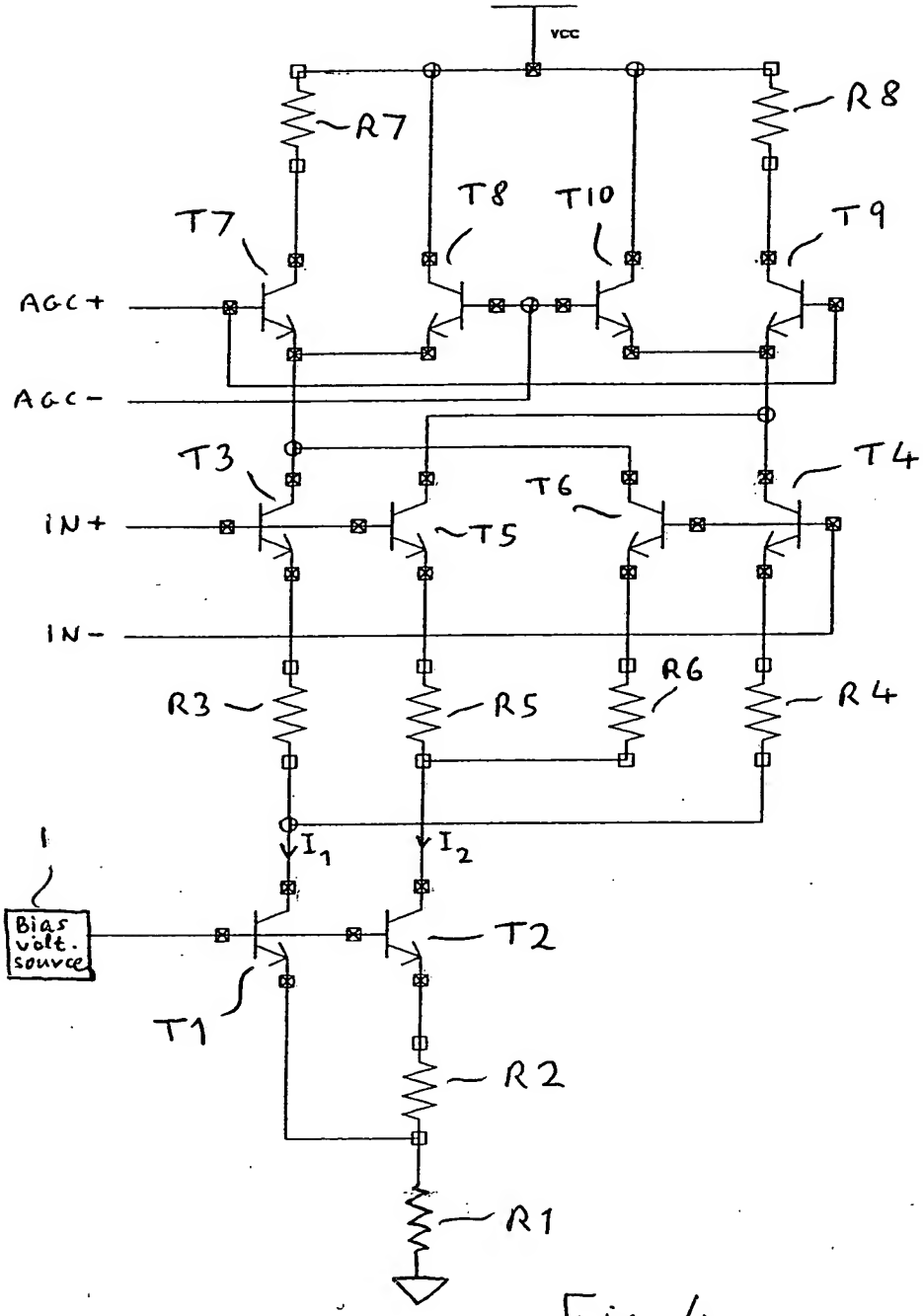
T2
$T1_1$
Bias voltage source
Vbias
$T1_2$
R2
R1

Fig 3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R8
T7
T8
T10
T9
AGC+
AGC-
T3
T6
T4
IN+
T5
IN-
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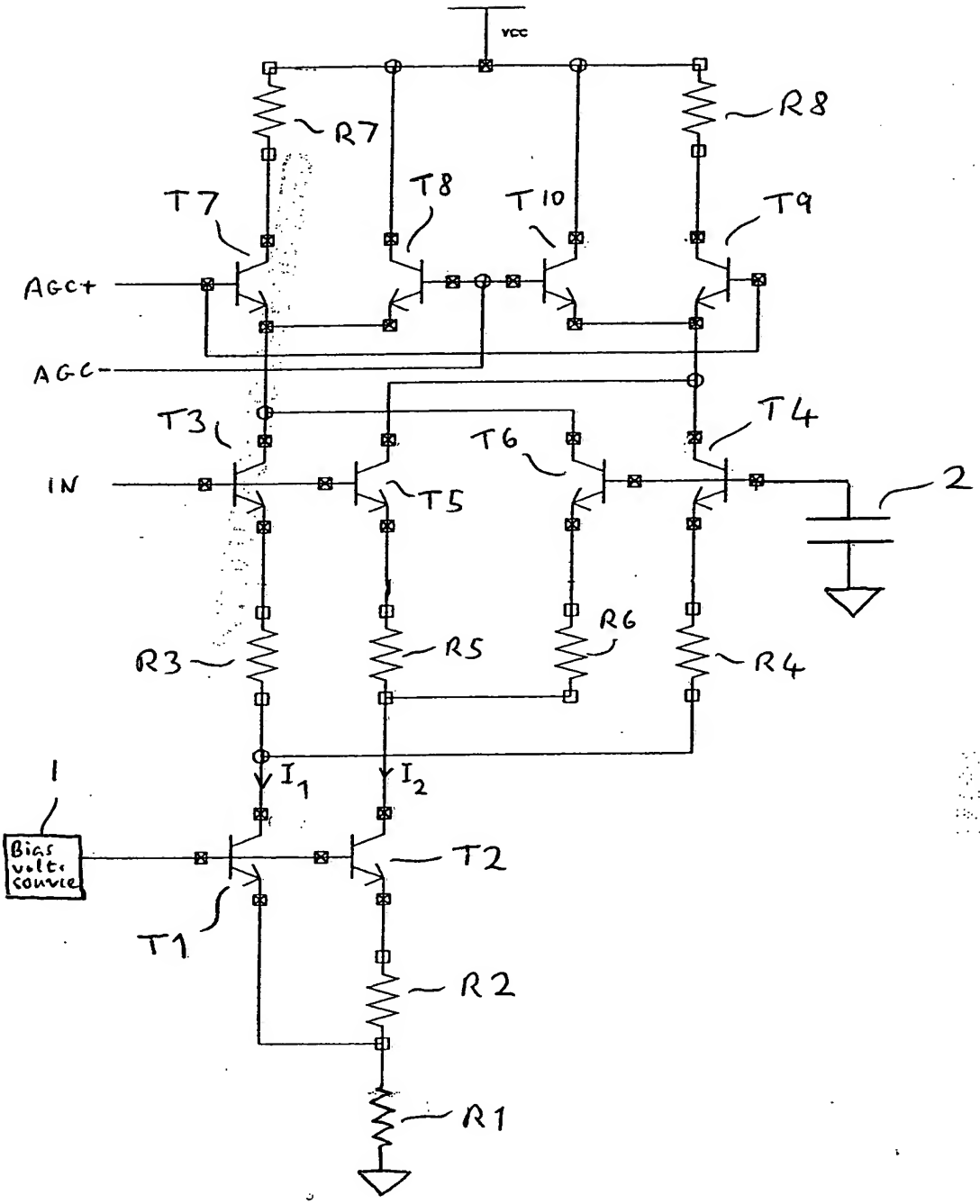
R5
R6
R4
I1
I2
I
Bias volt. source
T2
T1
R2
R1

Fig 4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T7
T8
T10
T9
AGC+
AGC-
T3
T4
T6
IN
T5
2
R3
R5
R6
R4
I1
I2
1
Bias volt. convie
T2
T1
R2
R1

Fig 5